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10/609,433	06/27/2003	Richard T. Oesterreicher	IVBU-0126	7933

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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,433	OESTERREICHER ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicants' Request for Continued Examination (RCE) filed on March 27, 2006 regarding application 10,609,433 filed on June 27, 2003.

2. Claims 1, 13 and 22-23 have been amended.

Claims 1-23 are pending under consideration.

3. ***Response to Remarks and Amendments***

Applicants' amendments and remarks have been fully and carefully considered.

Independent claims 1, 13 and 22-23 have been amended to include the new limitation of "**... core logic configured to dynamically accept algorithms that define or alter its operating characteristics without disrupting the operation of the media server ...**"

In response to this amendment, another iteration of claim analysis based on a previously relied on references (Olarig et al., US Patent Application Publication 2004/0024941, and Asano et al., US 6,327,614), and specifically addressing the newly added amendments, has been embarked. Refer to the corresponding sections of claim analysis for details.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. (US 6,327,614), and in view of Olarig et al. (US Patent Application Publication 2004/0024941).

As to claim 1, Asano et al. disclose **a method for reducing bus traversal** [Network Server Device and File management System Using Cache Associated with Network Interface Processor for Redirecting Requested Information between Connection Networks (title)] **in a media server** [figure 5 shows the medium server system] **comprising a host processor** [host machine, figure 5, 3], **a network interface** [figure 5 shows that the server device (1) interfaces to the network (2); figures 6 and 7 show the detailed block diagrams of the server device; figure 7 shows the network controller (24) which controls the network interface], **and a storage subsystem comprising one or more storage devices** [figure 6 shows a plurality of storage devices (14)], **the host processor and network interface being connected to a first input-output bus** [figure 5 shows that the host machine (3) and the server device being connected by the network (2), which may be an Ethernet bus or an ATM bus (column 4, lines 45-49), thus the first input-output bus], **the storage subsystem being connected to a second input-output bus** [figure 6 shows that the storage devices being connected by a parallel link (12), which is the internal bus (column 4, lines 50-58), thus the second input-output bus], **the first and second input-output buses being connected via a controller** [the corresponding controller is part of the network interface processor (figure 6, 11; figure 7); the connection between the first and the second buses is shown in figures 5, 6 and 7], **the method comprising**:

providing a hot-swappable adaptable cache [the corresponding adaptable cache comprises the Network Interface Processor unit (figure 6, 11; figure 7) including a Processor (figure 7, 21), a NIP Local Memory (figure 7, 22), a Network Controller (figure 7, 24), a Parallel Link Interface (figure 7, 25) and a ROM (figure 7, 23); the network interface local memory (figure 7, 22) function as a cache memory for storing a part of server data (abstract; column 2, lines 63-67; column 3, lines 18-40); a second instance of the corresponding adaptable cache comprises the Disk Interface Processor unit (figure 6, 13; figure 12) including a Processor (figure 12, 71), a DIP Local Memory (figure 12, 72), a SCSI Interface (figure 12, 74), a Parallel Link Interface (figure 12, 75) and a ROM (figure 12, 73); the DIP local memory (figure 12, 72) function as a cache memory for storing and providing a part of data requested by the NIP (column 8, lines 17-25); see below for explanation of hot-swappable limitation] **connected to the first input-output bus** [figures 5, 6, and 7], **said adaptable cache comprising a data interface** [the PCI BUS interface (figure 7, 26)], **core logic** [comprising the processor (figure 7, 21), the network controller (figure 7, 24) and the parallel link interface (figure 7, 25) and ROM (figure 7, 23)] **configured to dynamically accept algorithms that define or alter its operating characteristics** [figures 10-11 and 14 show the flowcharts of the algorithms that define the operating characteristics] **without disrupting the operation of the media server** [It is another object of the present invention to provide a server device with an efficient mechanism for transmission of information to a network (column 2, lines 57-59)], **and electronic storage media** [the NIP local memory (figure 7, 22) as well as the ROM (figure 7, 23)];

receiving a request for a media asset via a network [accept request from network controller, figure 10, 51]**, said request being received by the network interface** [when a request received from the network ... (column 3, lines 1-17; column 3, lines 18-40)];

receiving the request at the adaptable cache [column 3, lines 1-17; column 3, lines 18-40; figure 10];

processing the request by the adaptable cache [the network interface local processor (figure 7, 21) carries out a control processing such that a requested stored in the local memory (i.e., the cache, figure 7, 22) ... (column 3, lines 1-17; column 3, lines 18-40)], **wherein if the requested media asset is found on the electronic storage media, the media asset is returned to the user via the first bus and not the second bus** [column 5, lines 15-42; column 6, lines 9-22; figures 10, 11 and 14], **and wherein if the requested media asset is not found on the electronic storage media, the media asset is accessed from the storage subsystem and returned to the user via the second bus and first bus** [column 6, lines 23-30; figures 10, 11 and 14].

With respect to claim 1, Asano et al. do not mention **providing a cache that is hot-swappable**.

However, Olarig et al. teach in their invention "Method and Apparatus for Supporting Hot-Plug cache Memory" a method and apparatus to allow cache memory modules to be inserted and/or removed without shutting down the power of the system.

Hot insertion and removal of cache memory devices allows the system to continue its operation while replacing a faulty component, thus increase the throughput of the system.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicant's invention to recognize the benefits of hot-swappable cache memory components, as demonstrated by Olarig et al., and to incorporate it into the existing apparatus disclosed by Asano et al. to further enhance the throughput of the system.

As to claim 2, Asano et al. teach that **the request is received at the adaptable cache via the host processor** [a request from the network (figure 5, 2) to the server device (figure 5, 1) issued by the host machine (figure 5, 3) (column 15-16)].

As to claim 3, Asano et al. teach that **the request is receive' d at the adaptable cache directly from the network interface** [when a request received from the network at the network interface processor...(column 3, lines 1-17; column 3, lines 18-40).

As to claim 4, Asano et al. teach that **the adaptable cache is integrated with the network interface** [figure 7 shows that the cache is integrated as part of the network interface unit].

As to claim 5, Asano et al. teach that **the adaptable cache is integrated in the controller** [it is also possible to integrate the processor (i.e., the controller, figure 7, 21), the NIP local memory (i.e., the cache, figure 7, 22) and the PCI bus (figure 7, 26) into an ASIC called bridge chip (column 5, lines 1-12)].

As to claim 6, Asano et al. teach that **the adaptable cache monitors requests for media assets and if it is determined that the media asset should be cached, the media asset is transferred from one or more storage devices to the electronic storage media** [column 5, lines 15-42; column 6, lines 9-42; figures 10, 11 and 14].

As to claim 7, Asano et al. teach that **the adaptable cache monitors requests for media assets and if it is determined that the media should be cached, the adaptable cache notifies requesting applications that it can accept future requests for said media assets** [column 5, lines 15-42; column 6, lines 9-42; figures 10, 11 and 14. The information is provided in the form of HTTP protocol header, TCP header and IP header].

As to claim 8, Asano et al. teach that **the adaptable cache monitors requests for media assets and if it is determined that the media should be cached, the adaptable cache notifies the storage subsystem to disregard requests to deliver the media** [column 5, lines 15-42; column 6, lines 9-42; figures 10, 11 and 14. The information is provided in the form of HTTP protocol header, TCP header and IP header].

As to claim 9, Asano et al. teach that **if the requested media asset is not found on the electronic storage media, the adaptable cache stores the requested media asset on the electronic storage media** [column 6, lines 23-42; figures 10, 11 and 14].

As to claim 10, Asano et al. teach that **the adaptable cache integrates into the media server via an expansion card slot** [figure 7 shows that the components of the adaptable cache are modularized to be ready to be plugged into a PCI bus; further, it is

also possible to integrate the processor (i.e., the controller, figure 7, 21), the NIP local memory (i.e., the cache, figure 7, 22) and the PCI bus (figure 7, 26) into an ASIC called bridge chip (column 5, lines 1-12). Hence the adaptable cache can be made an expansion card to be plugged into a slot on a PCI bus].

As to claim 11, Asano et al. teach that **the adaptable cache integrates with native communications busses and protocols existing on the media server** [execute protocols in order to communications using HTTP and TCP/IP (column 1, lines 27-34; column 5, lines 15-20)].

As to claim 12, Asano et al. teach that **the adaptable cache utilizes the busses and protocols existing on the media server** [execute protocols in order to communications using HTTP and TCP/IP (column 1, lines 27-34; column 5, lines 15-20)].

As to claim 13, refer to "As to claim 1."

As to claim 14, Asano et al. teach that **the request is received at the adaptable cache via the second input-output bus** [this case is shown in figure 12, where the DIP local memory (72) within the disk interface processor serves as the cache memory. Note that the PCI bus (figure 12, 76) is directly connected to the parallel link via the parallel link interface (figure 12, 75) and the combined PCI bus and the parallel link can be considered as the second input-output bus].

As to claim 15, refer to "As to claim 10."

As to claim 16, refer to "As to claim 9."

As to claim 17, refer to "As to claim 6."

As to claim 18, refer to "As to claim 7."

As to claim 19, refer to "As to claim 8."

As to claim 20, refer to "As to claim 11."

As to claim 21, refer to "As to claim 12."

As to claim 22, refer to "As to claim 1."

As to claim 23, Asano et al. teach **a method of simulating passive monitoring of a bus by a first component** [the corresponding first component is the Network Interface Processor unit (figure 6, 11; figure 7) including a Processor (figure 7, 21), a NIP Local Memory (figure 7, 22), a Network Controller (figure 7, 24), a Parallel Link Interface (figure 7, 25) and a ROM (figure 7, 23); the network interface local memory (figure 7, 22) function as a cache memory for storing a part of server data (abstract; column 2, lines 63-67; column 3, lines 18-40); a second instance of the corresponding adaptable cache comprises the Disk Interface Processor unit (figure 6, 13; figure 12) including a Processor (figure 12, 71), a DIP Local Memory (figure 12, 72), a SCSI Interface (figure 12, 74), a Parallel Link Interface (figure 12, 75) and a ROM (figure 12, 73); the DIP local memory (figure 12, 72) function as a cache memory for storing and providing a part of data requested by the NIP (column 8, lines 17-25)] **in a computer device** [the service device (figure 5, 1)], **comprising**:

identifying a second component [the host machine (figure 5, 3)] **that transmits messages** [messages for requesting server data, using HTTP and TCP/IP protocols (column 1, lines 27-34; column 5, lines 15-20)] **to a third component** [one of the storage device (figure 6, 14)], **said messages desired to be monitored by the first**

component [that is what a server for], **wherein said first component comprises a hot-swappable adaptable cache** [the corresponding first component is the Network Interface Processor unit (figure 6, 11; figure 7) ; refer to "As to claim 1"], **said adaptable cache comprising a data interface** [the PCI BUS interface (figure 7, 26)], **core logic** [comprising the processor (figure 7, 21), the network controller (figure 7, 24) and the parallel link interface (figure 7, 25) and ROM (figure 7, 23)] **configured to dynamically accept algorithms that define or alter its operating characteristics** [figures 10-11 and 14 show the flowcharts of the algorithms that define the operating characteristics] **without disrupting the operation of the media server** [It is another object of the present invention to provide a server device with an efficient mechanism for transmission of information to a network (column 2, lines 57-59)], **and electronic storage media** [the NIP local memory (figure 7, 22) as well as the ROM (figure 7, 23)]; **and**

adapting the second component to address the message to both the third component and the first component [all three components, including the second component, must follow the HTTP and TCP/IP protocols for the communications among them (column 1, lines 27-34; column 5, lines 15-20)].

6. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Ofer, (US 6,189,080), "Minimum Read Rate Throughput in a Disk Cache System."

- Gotoh et al., (US 6,728,850), "Storage Control System."
- Anderson, (US 5,561,823), "Monitor System for Determining the Available Capacity of a Read Buffer and a Write Buffer in a Disk Drive System."
- Lasker et al., (US 5,586,291), "Disk Controller with Volatile and Non-Volatile Cache Memories."
- Lautzenheiser, (US 5,353,430), "Method of Operating a Cache system Including Determining an Elapsed Time or Amount of Data Written to Cache Prior to Writing to Main Storage."
- Singh, (US 6,665,704), "Bounding Delays and Reducing Threading Overheads in caching."
- Strothmann et al., (US Patent Application Publication 2004/0093288), "Methods and Systems for Pricing an Inventory Unit."
- Jilk, Jr. et al., (US Patent Application Publication 2002/0010746), "System, Method, Apparatus and Computer Program Product for Operating a Web Site by Electronic Mail."
- Hu et al., (US 6,535,518), "System for Bypassing a Server to Achieve Higher Throughput between Data Network and Data Storage System."
- Young et al., (US 5,761,458), "Intelligent Bus Bridge for Input/Output Subsystem in a Computer System."

Conclusion

7. Claims 1-23 are rejected as explained above.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

April 5, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
4|19|06